invention as required by 35 U.S.C. §103.

Claim 1 recites:

" A multiple semiconductor chip (multi-chip) module, comprising at least a power semiconductor chip and a control semiconductor chip each mounted directly on an electrically conductive heat sink, wherein said power semiconductor chip comprises a Silicon-On-Insulator (SOI) device and said control semiconductor ship comprises a bulk technology semiconductor device having no insulating layer between a device layer and a substrate thereof, and having said substrate connected to ground potential, and said power semiconductor chip and said control semiconductor chip are directly mounted on said electrically conductive heat sink without the use of a separate electrical insulation layer."

Uchida fails to teach or suggest, among other features, a multi-chip module "comprising at least a power semiconductor chip and a control semiconductor chip each mounted directly on an electrically conductive heat sink." On the contrary, **Uchida discloses a single semiconductor integrated circuit (IC) device** (i.e., a single chip) in which one semiconductor device (e.g., semiconductor device 130) is formed on a semiconductor substrate of the IC and another semiconductor device (e.g., semiconductor device 140) is formed on a silicon layer of the IC (see, e.g., col. 4, lines 44-55; FIG. 6; and col. 8, lines 8-45).

Uchida also fails to teach or suggest that "said power semiconductor chip comprises a Silicon-On-Insulator (SOI) device and said control semiconductor ship comprises a bulk technology semiconductor device having no insulating layer between a device layer and a substrate thereof." Rather, as is clearly shown, for example, in FIGS. 6 and 10A-10G of Uchida,

the semiconductor substrate and the silicon layer on which the semiconductor devices are formed are provided by a single SOI substrate comprising a silicon substrate 11, a buried insulating film 12, and a surface silicon layer 13.

The remaining references cited by the Examiner do not remedy the substantial deficiencies of Uchida.

Accordingly, because the cited references, taken alone or in any combination, fail to teach each and every feature of claim 1, Applicants respectfully submit that claim 1 is allowable.

Claims 2-7 depend from independent claim 1, and are, therefore, patentable for at least the reasons set forth above.

Accordingly, Applicant respectively submits that claims 1-7 are in condition for allowance.

If the Examiner believes that anything further is necessary to place the application in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

Dated:

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